AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior versions and listings of claims:

Listing of Claims:

1-5. (Cancelled)

6. (Currently Amended) A boundary scan test circuit comprising:

first and second multiplexers for receiving a shift/capture control signal at a control node of each of the first and second multiplexers, and for receiving first and second input signals, respectively;

first and second capture registers coupled to outputs of the first and second multiplexers, respectively;

first and second update registers coupled to outputs of the first and second capture registers, respectively;

third and fourth multiplexers coupled to outputs of the first and second update registers, respectively, for receiving a mode control signal at a control node of each of the third and fourth mulitplexers;

a buffer section coupled to outputs of the third and fourth multiplexers and to a pad for receiving an input/output signal; and

a first four-input multiplexer receiving the mode control signal at a control node of the first four-input multiplexer and having at least one input coupled to an input of the first multiplexer and at least one input coupled to an input of the third multiplexer.

7. (Original) The boundary scan test circuit of claim 6 further comprising means for enabling EXTEST and INTEST instructions to operate independently.

8. (Original) The boundary scan test circuit of claim 6 further comprising means for enabling EXTEST and INTEST instructions to operate simultaneously.

9. (Original) The boundary scan test circuit of claim 6 further comprising means for testing a bi-directional pad.

10. (Original) The boundary scan test circuit of claim 6 further comprising a second four-input multiplexer having at least one input coupled to an input of the first four-input multiplexer.

11. (Original) The boundary scan test circuit of claim 6 further comprising a second four-input multiplexer having at least one input coupled to an output of the first four-input multiplexer.

12. (Previously presented) The boundary scan test circuit of claim 6 wherein an output of the second four-input multiplexer provides a control signal for the first four-input multiplexer.

13. (Currently Amended) A boundary scan test circuit comprising:

a first multiplexer circuit for receiving a core logic input signal and a shift/capture control signal;

a capture register circuit coupled to an output of the first multiplexer circuit;

an update register circuit coupled to an output of the capture register circuit;

a second multiplexer circuit coupled to an output of the update register circuit for receiving a mode control signal at a control node of the second multiplexer circuit; and

a buffer coupled to an output of the second multiplexer circuit and to a pad for receiving an input/output signal.

14. (Previously presented) The boundary scan test circuit of claim 13 further comprising circuitry for enabling EXTEST and INTEST instructions to operate independently.

15. (Previously presented) The boundary scan test circuit of claim 13 further comprising circuitry for enabling EXTEST and INTEST instructions to operate simultaneously.

16. (Previously presented) The boundary scan test circuit of claim 13 further comprising circuitry for testing a bi-directional pad.

17. (Previously presented) The boundary scan test circuit of claim 13 wherein the first multiplexer circuit comprises a four-input multiplexer.

18. (Previously presented) The boundary scan test circuit of claim 13 wherein the second multiplexer circuit comprises a four-input multiplexer.

19. (Previously presented) The boundary scan test circuit of claim 13 wherein an output of the fourth multiplexer in the second multiplexer circuit provides a control signal for an input of the four-input multiplexer.

20. (Previously presented) The boundary scan test circuit of claim 13 further comprising a logic circuit coupled between the first and second multiplexer circuits.

21. (Previously presented) The boundary scan test circuit of claim 13 wherein the capture register circuit provides a scan output signal.

22. (Previously presented) The boundary scan test circuit of claim 13 wherein the update register circuit receives an update input signal.